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A conductive mesh bias connection for an array of elevated active pixel sensors

Abstract:

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An array of active pixel sensors. The array of active pixel sensors includes a substrate (200). An interconnect structure (210) is formed adjacent to the substrate. The interconnect structure (210) includes a plurality of conductive vias (212, 214, 216, 218). A plurality of photo sensors are formed adjacent to the interconnect structure (210). Each photo sensor includes a pixel electrode (222, 224, 226). Each pixel electrode (222, 224, 226) is electrically connected to the substrate (200) through a corresponding conductive via (214, 216, 218). An I-layer (220) is formed over each of the pixel electrodes. The array of active pixel sensors further includes a conductive mesh (240) formed adjacent to the photo sensors. An inner surface of the conductive mesh (240) is electrically and physically connected to the photo sensors, and electrically connected to the substrate through a conductive via (212). The conductive mesh (240) providing light shielding between photo sensors thereby reducing cross-talk between the photo sensors. The conductive mesh (240) includes apertures that align with at least one of the pixel electrodes of the photo sensors.

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(54) **A conductive mesh bias connection for an array of elevated active pixel sensors**

(57) An array of active pixel sensors. The array of active pixel sensors includes a substrate (200). An interconnect structure (210) is formed adjacent to the substrate. The interconnect structure (210) includes a plurality of conductive vias (212, 214, 216, 218). A plurality of photo sensors are formed adjacent to the interconnect structure (210). Each photo sensor includes a pixel electrode (222, 224, 226). Each pixel electrode (222, 224, 226) is electrically connected to the substrate (200) through a corresponding conductive via (212, 214, 216, 218).

An I-layer (220) is formed over each of the pixel electrodes. The array of active pixel sensors further includes a conductive mesh (240) formed adjacent to the photo sensors. An inner surface of the conductive mesh (240) is electrically and physically connected to the photo sensors, and electrically connected to the substrate through a conductive via (212). The conductive mesh (240) providing light shielding between photo sensors thereby reducing cross-talk between the photo sensors. The conductive mesh (240) includes apertures that align with at least one of the pixel electrodes of the photo sensors.

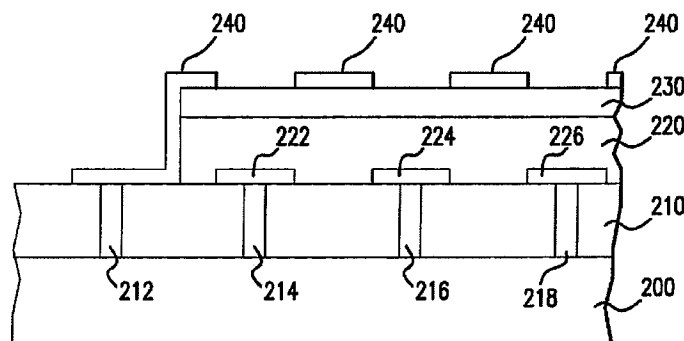


FIG.2

Description

FIELD OF INVENTION

[0001] This invention relates generally to photo diode active pixel sensors. In particular, it relates to a conductive mesh bias connection for an array of elevated active pixel sensors which provides light shielding between the active pixel sensors.

BACKGROUND

[0002] An array of image sensors or light sensitive sensors detect the intensity of light received by the image sensors. The image sensors typically generate electronic signals that have amplitudes that are proportionate to the intensity of the light received by the image sensors. The image sensors can convert an optical image into a set of electronic signals. The electronic signals may represent intensities of colors of light received by the image sensors. The electronic signals can be conditioned and sampled to allow image processing.

[0003] Integration of the image sensors with signal processing circuitry is becoming more important because integration enables miniaturization and simplification of imaging systems. Integration of image sensors along with analog and digital signal processing circuitry allows electronic imaging systems to be low cost, compact and require low power consumption.

[0004] Historically, image sensors have predominantly been charged coupled devices (CCDs). CCDs are relatively small and can provide a high-fill factor. However, CCDs are very difficult to integrate with digital and analog circuitry. Further, CCDs dissipate large amounts of power and suffer from image smearing problems.

[0005] An alternative to CCD sensors are active pixel sensors. Active pixel sensors can be fabricated using standard CMOS processes. Therefore, active pixel sensors can easily be integrated with digital and analog signal processing circuitry. Further, CMOS circuits dissipate small amounts of power.

[0006] Figure 1 shows a cross-section of a prior art array of image sensors. This array of image sensors includes PIN diode sensors located over a substrate 10. An interconnection structure 12 electrically connects an N-layer 14 of the PIN diodes to the substrate 10. An I-layer 16 is formed over the N-layer 14. A P-layer 18 is formed over the I-layer 16. The P-layer 18, the I-layer 16 and the N-layer 14 form the array of PIN diode sensors. A first conductive via 20 electrically connects a first diode sensor to the substrate 10, and a second conductive via 22 electrically connects a second diode sensor to the substrate 10. A transparent conductive layer 24 is located over the array of diode sensors. A conductive lead 26 is connected to the transparent conductive layer 24. The conductive lead 26 is connected to a bias voltage which allows biasing of the P-layer 18 of the array of PIN diode sensors to a selected voltage potential.

[0007] A limitation of the image sensor structure of Figure 1 is the lack of shielding between the image sensors. Light received by a given sensor is also received by a neighboring sensor because there is no shielding of light between neighboring sensors. Light received by a given image sensor will also effect neighboring image sensors because current can flow through the N-layer 14 between neighboring image sensors. Charge can flow between the image sensors especially when the light intensity of the received light varies greatly between neighboring image sensors. The P-layer 18, the I-layer 16 and the N-layer 14 are shared by neighboring image sensors. A trench 28 is formed to provide some isolation between the image sensors by increasing the resistance between the N-layers sections of neighboring image sensors.

[0008] Another limitation of the image sensor structure of Figure 1 is the electrical connection between the conductive lead 26 and the transparent conductive layer 24. The transparent conductive layer 24 must be electrically conductive to allow biasing of the PIN diodes, and must be transparent to allow the PIN diodes to receive light. Generally, it is very difficult to bond to the types of materials that must be used to form the transparent conductive layer 24. Therefore, the conductive lead 26 must be attached to the transparent conductive layer 24 with the aid of some type of clamp or support structure. The result being an electrical connection which is not reliable and which is expensive to produce.

[0009] It is desirable to have an array of active pixel sensors formed adjacent to a substrate in which light received by an active pixel sensors of the array is shielded from the other active pixel sensors of the array. That is, it is desirable that isolation exist between the active pixel sensors which reduces the effect that light received by an active pixel sensor of the array has on the other active pixel sensors of the array. It is also desirable that the active pixel sensor array include a conductive layer that provides a bias voltage to the array of active pixel sensors, and that is reliably electrically connected to a pixel sensor bias voltage which originates on the substrate.

SUMMARY OF THE INVENTION

[0010] The present invention is an array of elevated active pixel sensors formed adjacent to a substrate that includes a conductive mesh that is reliably electrically connected to the pixel sensors and a pixel sensor bias voltage which is located on the substrate. The conductive mesh provides shielding of light received by each pixel sensor from the other pixel sensors. That is, the conductive mesh provides isolation between the active pixel sensors which reduces the effect that light received by an active pixel sensor of the array has on the other active pixel sensors of the array. The conductive mesh provides a bias voltage to the array of active pixel sensors. The substrate can be a CMOS substrate which in-

cludes image processing circuitry.

[0011] A first embodiment of this invention includes an array of active pixel sensors. The array of active pixel sensors includes a substrate. An interconnect structure is formed adjacent to the substrate. The interconnect structure includes a plurality of conductive vias. A plurality of photo sensors are formed adjacent to the interconnect structure. Each photo sensor includes a pixel electrode. Each pixel electrode is electrically connected to the substrate through a corresponding conductive via. An I-layer is formed over each of the pixel electrodes. The array of active pixel sensors further includes a conductive mesh formed adjacent to the photo sensors. An inner surface of the conductive mesh is electrically and physically connected to the photo sensors, and electrically connected to the substrate through a conductive via.

[0012] A second embodiment of this invention is similar to the first embodiment. The second embodiment includes the conductive mesh providing light shielding between photo sensors thereby reducing cross-talk between the photo sensors.

[0013] A third embodiment of this invention is similar to the second embodiment. The third embodiment includes apertures of the conductive mesh aligning with at least one of the pixel electrodes of the photo sensors.

[0014] A fourth embodiment of this invention is similar to the first embodiment, but further includes a P-layer formed between the I-layer and the conductive mesh. The inner surface of the conductive mesh is electrically connected to the P-layer and the interconnect structure.

[0015] Other aspects and advantages of the present invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] Figure 1 shows a cross-section of a prior art array of image sensors.

[0017] Figure 2 shows an embodiment of the invention.

[0018] Figure 3 shows a top view of an embodiment of the invention.

[0019] Figure 4 shows another embodiment of the invention.

[0020] Figure 5 shows pixel electrodes deposited on the pixel interconnect structure.

[0021] Figure 6 shows an I-layer and a P-layer deposited over a plurality of pixel electrodes.

[0022] Figure 7 shows the P-layer and the I-layer selectively etched to allow access to a conductive via.

[0023] Figure 8 shows a conductive layer deposited over the P-layer which provides an electrical connection between the P-layer and the interconnection structure.

[0024] Figure 9 shows the transparent conductive layer having been etched according to a predetermined

pattern.

DETAILED DESCRIPTION

[0025] As shown in the drawings for purposes of illustration, the invention is embodied in an array of elevated active pixel sensors formed adjacent to a substrate that includes a conductive mesh that is reliably electrically connected to the pixel sensors and a pixel sensor bias voltage which is located on the substrate. The conductive mesh provides shielding of light received each pixel sensor from the other pixel sensors. That is, the conductive mesh provides isolation between the active pixel sensors which reduces the effect that light received by an active pixel sensor of the array has on the other active pixel sensors of the array. The conductive mesh provides a bias voltage to the array of active pixel sensors.

[0026] Figure 2 shows a first embodiment of the invention. This embodiment includes a substrate 200. The substrate 200 includes electronic circuitry. An interconnection structure 210 is formed adjacent to the substrate 200. Pixel electrodes 222, 224, 226 are formed adjacent to the interconnection structure 210. Each pixel sensor of an array of pixel sensors includes an individual pixel electrode 222, 224, 226. An I-layer 220 is formed adjacent to the pixel electrodes 222, 224, 226. A P-layer 230 is formed adjacent to the I-layer 220. A conductive mesh 240 is formed adjacent to the P-layer 230. A first pixel electrode 222 of a first pixel sensor is electrically connected to the substrate 200 through a first conductive via 214. A second pixel electrode 216 of a second pixel sensor is electrically connected to the substrate 200 through a second conductive via 216. A third pixel electrode 226 of a third pixel sensor is electrically connected to the substrate 200 through a third conductive via 218. The conductive mesh 240 is electrically connected to the substrate 200 through a fourth conductive via 212.

[0027] Figure 3 shows a top-view of an embodiment of the invention. The top-view more clearly depicts the physical characteristics of the conductive mesh 240. The conductive mesh 240 include apertures 310 which align with the pixel electrodes 222, 224, 226 of the pixel sensors. The conductive mesh 240 provides shielding of light between the pixel sensors. The apertures 310 within the conductive mesh 240 allow light to be received by pixel sensors which align with the apertures 310 while shielding the received light from other pixel sensors.

[0028] The conductive mesh 240 is physically and electrically connected to the P-layer 230. The conductive mesh 240 is also electrically connected to the substrate 200 through the fourth conductive via. The conductive mesh 240 is driven to a bias voltage potential by electronic circuitry within the substrate 200. The bias voltage potential biases the pixel sensors.

[0029] The pixel sensors conduct charge when the pixel sensors receive light. The substrate 200 generally includes sense circuitry and signal processing circuitry.

The sense circuitry senses how much charge the pixel sensors have conducted. The amount of charge conducted represents the intensity of light received by the pixel sensors. Generally, the substrate 200 can be CMOS (complementary metal oxide silicon), BiCMOS or Bipolar. The substrate 200 can include various types of substrate technology including charged coupled devices.

[0030] Typically, the interconnection structure 210 is a standard CMOS interconnection structure. The structure and methods of forming this interconnection structure 210 are well known in the field of electronic integrated circuit fabrication. The interconnection structure 210 can be a subtractive metal structure, or a single or dual damascene structure.

[0031] The conductive vias 214, 216, 218 pass through the pixel interconnect structure 210 and electrically connect the pixel electrodes 222, 224, 226 to the substrate 200. The fourth conductive via 212 passes through the pixel interconnect structure 210 and provides a reliable electrical connection between the conductive mesh 240 and the substrate 200. Typically, the conductive vias 212, 214, 216, 218 are formed from tungsten. Tungsten is generally used during fabrication because tungsten can fill high aspect ratio holes. That is, tungsten can be used to form narrow and relatively long interconnections. Typically, the conductive vias 212, 214, 216, 218 are formed using a chemical vapor deposition (CVD) process. Other materials which can be used to form the conductive vias 212, 214, 216, 218 include copper, aluminum or any other electrically conductive material.

[0032] The pixel electrodes 222, 224, 226 are generally formed from a doped semiconductor. The doped semiconductor can be an N-layer of amorphous silicon. The pixel electrodes 222, 224, 226 must be thick enough, and doped heavily enough that the pixel electrodes 222, 224, 226 do not fully deplete when biased during operation. The pixel electrodes 222, 224, 226 are typically doped with phosphorous.

[0033] The pixel electrodes 222, 224, 226 are typically deposited using plasma etched chemical vapor deposition (PECVD). The PECVD is performed with a phosphorous containing gas. The phosphorous gas can be PH_3 . A silicon containing gas is included when forming amorphous silicon pixel electrodes.

[0034] An N-layer of amorphous silicon is typically used when forming the pixel electrodes 222, 224, 226 of the PIN diode active pixel sensors. However, the diode active pixel sensors can include an NIP sensor configuration. In this case, the pixel electrodes 222, 224, 226 are formed from a P-layer, and the P-layer 230 of Figure 2 is replaced with an N-layer.

[0035] The I-layer 220 is generally formed from a hydrogenated amorphous silicon. The I-layer 220 can be deposited using a PECVD or a reactive sputtering process. The PECVD process must include a silicon containing gas. The deposition should be at a low enough tem-

perature that hydrogen is retained within the film. The I-layer 220 is approximately one micron thick.

[0036] The P-layer 230 is generally formed from amorphous silicon. Typically, the P-layer 230 is doped with Boron. The P-layer 230 can be deposited using PECVD. The PECVD is performed with a Boron containing gas. The Boron containing gas can be B_2H_6 . A silicon containing gas is included when forming an amorphous silicon P-layer 230. The P-layer 230 thickness must generally be controlled to ensure that the P-layer 230 does not absorb too much short wavelength (blue) light.

[0037] Another embodiment of the invention does not include a P-layer 230. The P-layer 230 can be eliminated with proper selection of the composition of the material within the conductive mesh 240, and proper selection of the doping levels of the pixel electrodes 222, 224, 226. For this embodiment, the conductive mesh 240 provides a conductive connection between a top surface of the I-layer 220 of the pixel sensors and the interconnection structure 210.

[0038] As previously described, the pixel electrodes 222, 224, 226, the I-layer 220 and the P-layer 230 are generally formed from amorphous silicon. However, the pixel electrodes 222, 224, 226, the I-layer 220 and the P-layer 230 can also be formed from amorphous carbon, amorphous silicon carbide, amorphous germanium, or amorphous silicon-germanium. It should be understood that this list is not exhaustive.

[0039] The conductive mesh 240 provides a conductive connection between the P-layer 230 and the interconnection structure 210. Light must pass through the apertures of the conductive mesh 240 and is received by the pixel sensors. The conductive mesh 240 is formed from an opaque conductive material. Materials that can be used to form the conductive mesh 240 include aluminum, tungsten or copper. It is to be understood that this list is not exhaustive.

[0040] The conductive mesh 240 can be formed by depositing the conductive mesh material 240 by a sputtering process, and then etching the conductive mesh material according to a mesh pattern to form the conductive mesh 240. Deposition through sputtering and etching according to a pattern are well known in the art of integrated circuit fabrication.

[0041] Figure 4 shows another embodiment of the invention. This embodiment includes I-layer sections 410 rather than a single I-layer 220. That is, each pixel sensor includes a separate I-layer section 410 rather than a single I-layer 220 which is formed as a part of many pixel sensors. Like the pixel electrodes 212, 214, 216, the I-layer sections can be etched according to a predetermined pattern.

[0042] Figures 5-9 show processing steps which can be used to fabricate the embodiments shown in Figure 2, Figure 3 and Figure 4.

[0043] Figure 5 shows a substrate 200 with an interconnection structure 210 formed over the substrate 200.

Pixel electrodes 222, 224, 226 are formed over the interconnection structure 210. The structure and methods of forming this interconnection structure 210 are well known in the field of electronic integrated circuit fabrication. The interconnection structure 210 can be a subtractive metal structure, or a single or dual damascene structure.

[0044] The interconnection structure 210 includes conductive vias 212, 214, 216, 218 that are generally formed from tungsten. Tungsten is generally used because during fabrication, tungsten can fill high aspect ratio holes. That is, tungsten can be used to form narrow and relatively long interconnections. Typically, the conductive vias 212, 214, 216, 218 are formed using a chemical vapor deposition (CVD) process. Other materials which can be used to form the conductive vias 212, 214, 216, 218 include copper, aluminum or any other electrically conductive material.

[0045] The pixel electrodes 222, 224, 226 are deposited on the interconnection structure 210. A pixel electrode layer is first deposited over the interconnection structure 210. Then the pixel electrode layer is etched according to a predetermined pattern forming the pixel electrodes 222, 224, 226. An individual pixel electrode 222, 224, 226 is formed for each pixel sensor. The pixel electrodes 222, 224, 226 can be implemented with N-layer sections. Alternatively, the pixel electrodes 222, 224, 226 can be implemented with a conductive nitride, like, titanium nitride.

[0046] The pixel electrodes 222, 224, 226 are typically deposited using PECVD. The PECVD is performed with a phosphorous containing gas. The phosphorous containing gas can be PH_3 . A silicon containing gas, such as Si_2H_6 or SiH_4 , is included when forming amorphous silicon pixel electrodes. The predetermined pixel electrode pattern is formed through a wet or dry etch of the deposited pixel electrode material.

[0047] Figure 6 shows an I-layer 220 and a P-layer 230 deposited over the plurality of pixel electrodes 222, 224, 226. The I-layer 220 is generally deposited using a PECVD or reactive sputtering process. The PECVD must include a silicon containing gas. The deposition should be at a low enough temperature that hydrogen is retained within the film. The P-layer 230 can also be deposited using PECVD. The PECVD is performed with a Boron containing gas. The Boron containing gas can be B_2H_6 . A silicon containing gas is included when forming an amorphous silicon P-layer 230.

[0048] Figure 7 shows the P-layer 230 and the I-layer 220 having been etched to provide access to the fourth conductive via 212. The fourth conductive via 212 is electrically connected to a reference voltage on the substrate 200 which is used to bias the array of pixel sensors.

[0049] Figure 8 shows a conductive layer 810 deposited over the P-layer 230 which provides an electrical connection between the P-layer 230 and the fourth conductive via 212. The conductive layer 810 is formed from

an opaque conductive material. Materials that can be used to form the conductive layer 810 include aluminum, tungsten or copper. It is to be understood that this list is not exhaustive.

5 [0050] The conductive layer 810 is generally deposited through reactive sputtering. However, the conductive layer 810 can also be grown by evaporation, or deposited through chemical vapor deposition or plasma vapor deposition.

10 [0051] Figure 9 shows the conductive layer 810 having been etched according to a predetermined pattern forming the conductive mesh 240. Etching of conductive materials is well known in the art of semiconductor processing.

15 [0052] Although specific embodiments of the invention have been described and illustrated, the invention is not to be limited to the specific forms or arrangements of parts so described and illustrated. The invention is limited only by the claims.

Claims

1. An array of active pixel sensors comprising:

25 a substrate (200);
an interconnect structure (210) adjacent to the substrate, the interconnect structure comprising a plurality of conductive vias;
a plurality of photo sensors adjacent to the interconnect structure, each photo sensor comprising:

30 a pixel electrode (222, 224, 226), the pixel electrode electrically connected to the substrate through a corresponding conductive via (214, 216, 218);
an I-layer (220) formed over the pixel electrode;

40 the array of active pixel sensors further comprising:
a conductive mesh (240) formed adjacent to the photo sensors, an inner surface of the conductive mesh electrically and physically connected to the photo sensors, and electrically connected to the substrate through a conductive via (212).

50 2. The active pixel sensor as recited in claim 1, wherein the conductive mesh (240) comprises apertures in which each aperture aligns with at least one of the pixel electrodes of the photo sensors.

55 3. The active pixel sensor as recited in claim 1, wherein each pixel electrode (222, 224, 226) comprises an N-layer.

4. The active pixel sensor as recited in claim 1, where-
in the interconnect structure (210) electrically inter-
connects the pixel electrodes to the substrate.
5. The active pixel sensor as recited in claim 1, where- 5
in the I-layer (220) and the pixel electrodes (222,
224, 226) each comprise amorphous silicon.
6. The active pixel sensor as recited in claim 1, further 10
comprising a P-layer (230) formed between the I-
layer (220) and the conductive mesh (240), the in-
ner surface of the conductive mesh physically con-
nected to the P-layer, the I-layer, and electrically
connected to the substrate through a conductive
via. 15
7. The active pixel sensor as recited in claim 6, where-
in the P-layer (230) comprises amorphous silicon.
8. The active pixel sensor as recited in claim 1, where- 20
in the inner surface of the conductive mesh (240) is
electrically connected to the substrate through at
least one tungsten plug (212).
9. The active pixel sensor as recited in claim 1, where- 25
in the conductive mesh (240) comprises indium tin
oxide.
10. The active pixel sensor as recited in claim 1, where- 30
in the substrate (200) is selected from a group in-
cluding CMOS, active circuits which sense charge
accumulated by the photo sensors due to the photo
sensors receiving light, and charge coupled devic-
es. 35
11. The active pixel sensor as recited in claim 1, where-
in each pixel electrode (222, 224, 226) comprises a
P-layer.
12. The active pixel sensor as recited in claim 1, where- 40
in each pixel electrode (222, 224, 226) comprises a
conductive metal.

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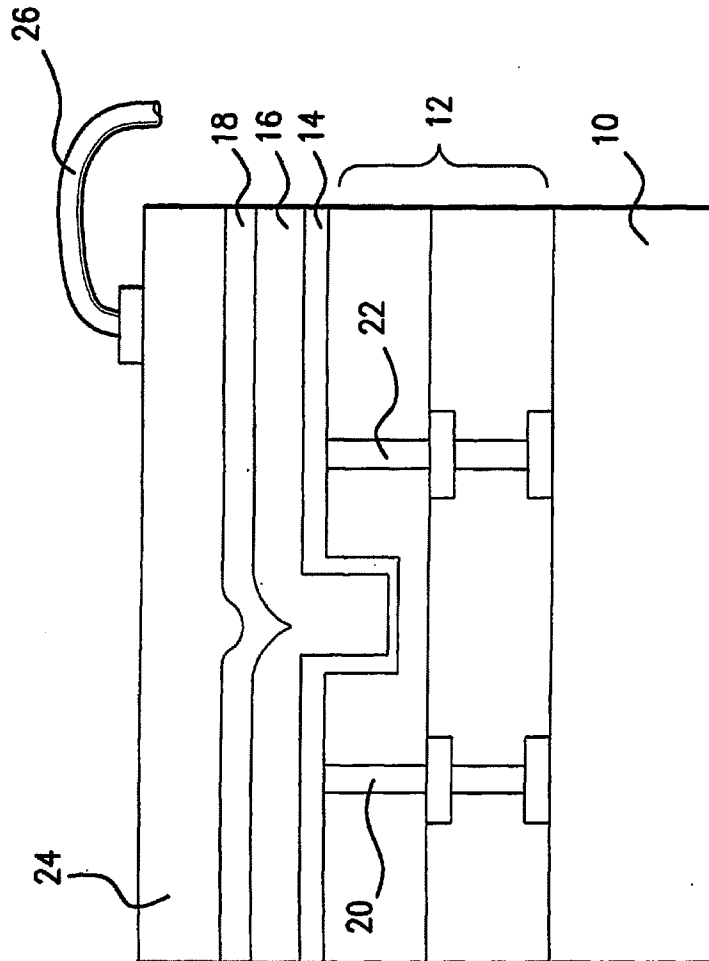


FIG. 1
PRIOR ART

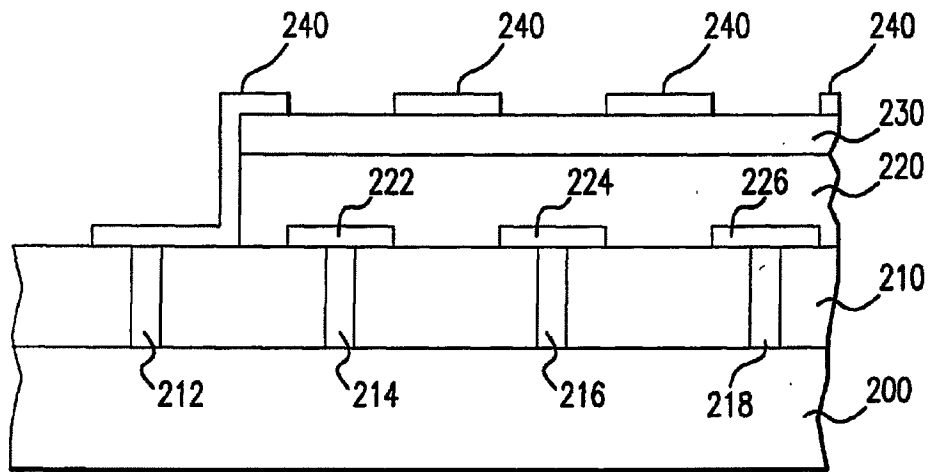


FIG.2

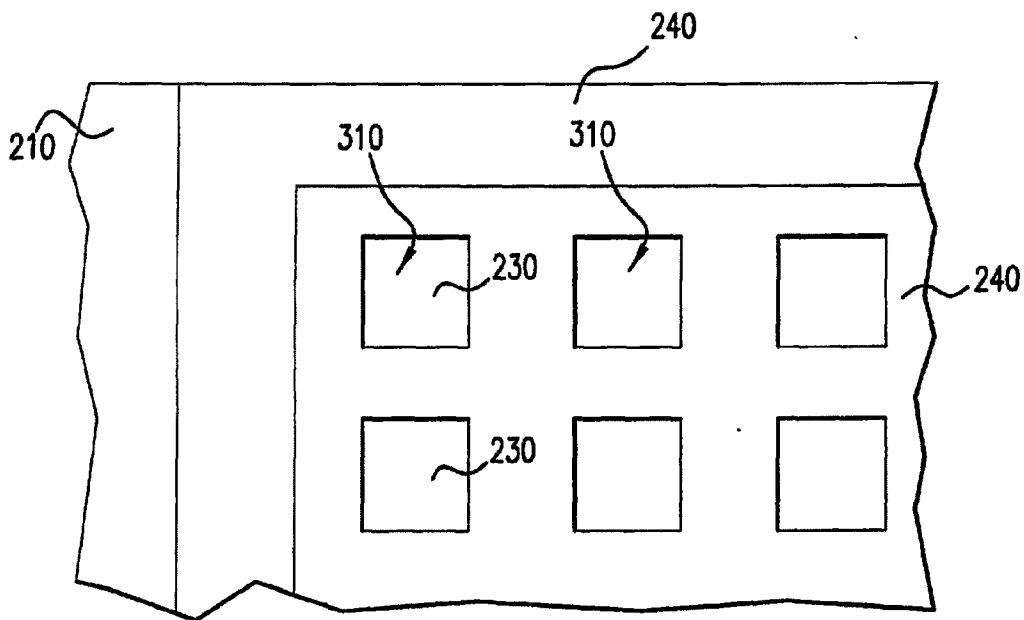


FIG.3

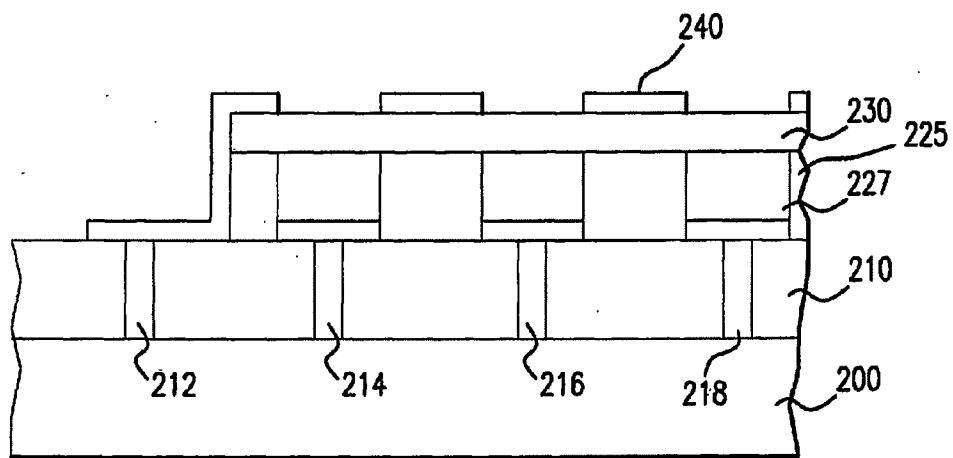


FIG.4

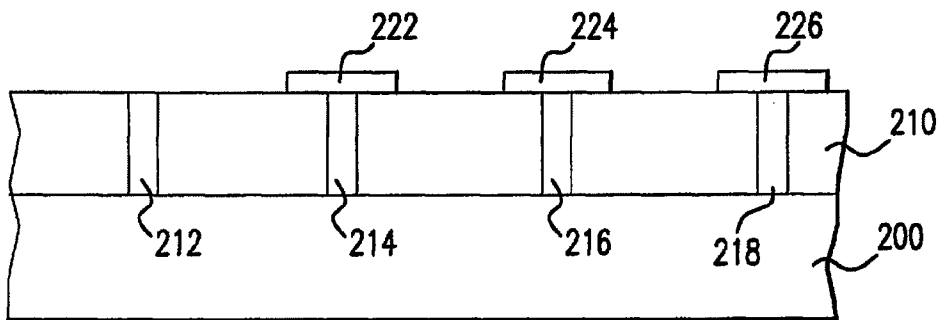


FIG. 5

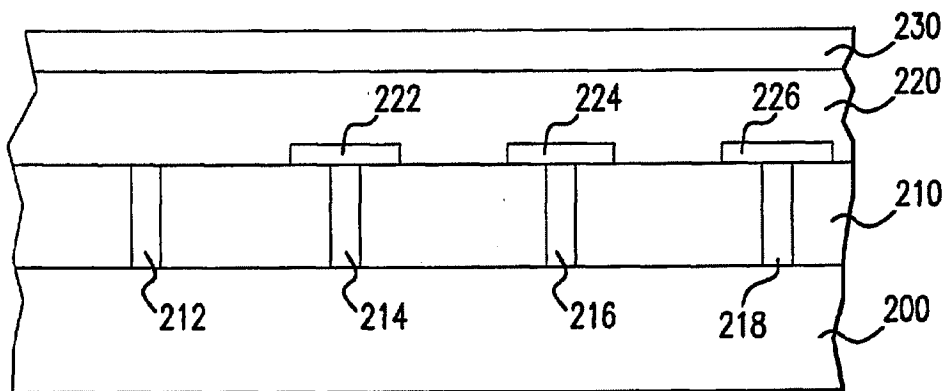


FIG. 6

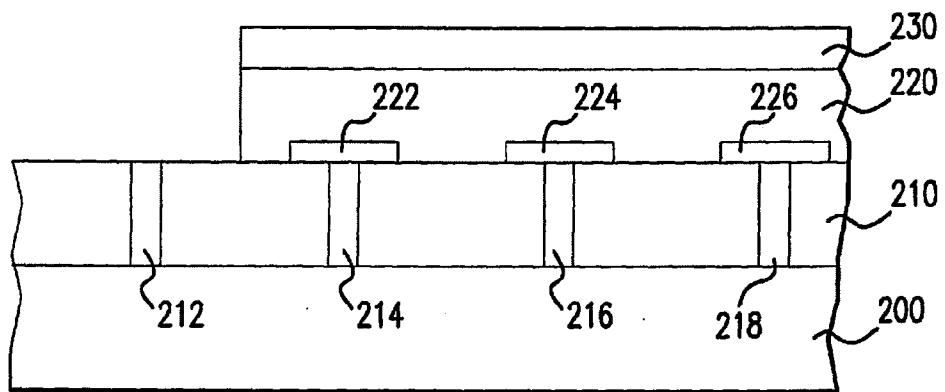


FIG. 7

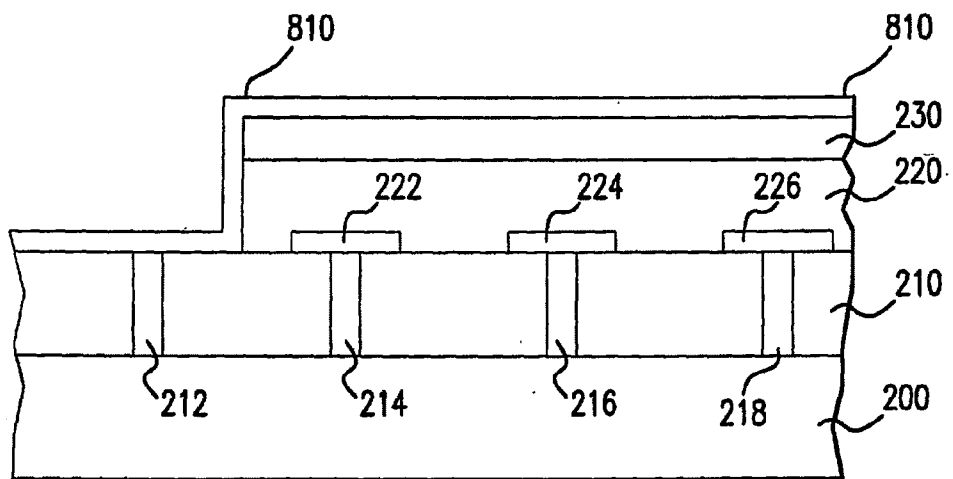


FIG. 8

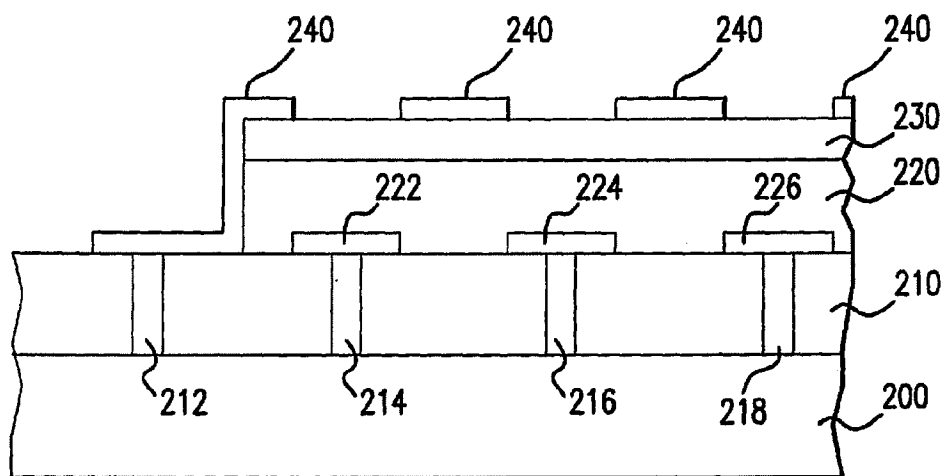


FIG.9